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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Laurence B. Boucher et al.		Ser. No:	09/067,544
Filing Date:	April 27, 1998	Examiner:	Unknown
Atty. Docket No:	ALA-002	GAU:	Unknown

For: INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING

January 5, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

Information Disclosure Statement per 37 C.F.R. §1.98

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicants bring the following documents to the Examiner's attention, copies of which are enclosed. A form PTO-1449 listing these documents is also enclosed.

Citation of these documents shall not be construed as an admission that the documents are prior art with respect to the instant invention, a representation that a search has been made, or an admission that the information cited herein is, or is considered to be, material to patentabilty as defined in 37 C.F.R. § 1.56(b).

Patent Documents

1. U.S. Patent No. 4,991,133 to Davis et al. entitled SPECIALIZED COMMUNICATIONS PROCESSOR FOR LAYERED PROTOCOLS.
2. U.S. Patent No. 5,163,131 to Row et al. entitled PARALLEL I/O NETWORK FILE SERVER ARCHITECTURE.
3. U.S. Patent No. 5,212,778 to Dally et al. entitled MESSAGE DRIVEN PROCESSOR IN A CONCURRENT COMPUTER.
4. U.S. Patent No. 5,289,580 to Latif et al. entitled PROGRAMMABLE MULTIPLE I/O INTERFACE CONTROLLER.

5. U.S. Patent No. 5,303,344 to Yokoyama et al. entitled PROTOCOL PROCESSING APPARATUS FOR USE IN INTERFACING NETWORK CONNECTED COMPUTER SYSTEMS UTILIZING SEPARATE PATHS FOR CONTROL INFORMATION AND DATA TRANSFER

6. U.S. Patent No. 5,412,782 to Hausman et al. entitled PROGRAMMED I/O ETHERNET ADAPTER WITH EARLY INTERRUPTS FOR ACCELERATING DATA TRANSFER.

7. U.S. Patent No. 5,485,579 to Hitz et al. entitled MULTPLE FACILITY OPERATING SYSTEM ARCHITECTURE

8. U.S. Patent No. 5,506,966 to Ban entitled SYSTEM FOR MESSAGE TRAFFIC CONTROL UTILIZING PRIORITIZED MESSAGE CHAINING FOR QUEUEING CONTROL ENSURING TRANSMISSION/RECEPTION OF HIGH PRIORITY MESSAGES.

9. U.S. Patent No. 5,511,169 to Suda entitled DATA TRANSMISSION APPARATUS AND A COMMUNICATION PATH MANAGEMENT METHOD THEREFOR.

10. U.S. Patent No. 5,548,730 to Young et al. entitled INTELLIGENT BUS BRIDGE FOR INPUT/OUTPUT SUBSYSTEMS IN A COMPUTER SYSTEM.

11. U.S. Patent No. 5,558,121 to Reddin et al. entitled PARALLEL COMPUTER HAVING MAC-RELAY LAYER SNOOPED TRANSPORT HEADER TO DETERMINE IF A MESSAGE SHOULD BE ROUTED DIRECTLY TO TRANSPORT LAYER DEPENDING UPON ITS DESTINATION.

12. U.S. Patent No. 5,590,328 to Seno et al. entitled PROTOCOL PARALLEL PROCESSING APPARATUS HAVING A PLURALITY OF CPUS ALLOCATED TO PROCESS HIERARCHICAL PROTOCOLS.

13. U.S. Patent No. 5,592,622 to Isfeld et al. entitled NETWORK INTERMEDIATE SYSTEM WITH MESSAGE PASSING ARCHTECTURE.

14. U.S. Patent No. 5,634,099 to Andrews et al. DIRECT MEMORY ACCESS UNIT FOR TRANSFERRING DATA BETWEEN PROCESSOR MEMORIES IN MULTIPROCESSING SYSTEMS.

15. U.S. Patent No. 5,642,482 to Pardillos entitled SYSTEM FOR NETWORK TRANSMISSION USING A COMMUNICATION COPROCESSOR COMPRISING A MICROPROCESSOR TO IMPLEMENT PROTOCOL LAYER AND A MICROPROCESSOR TO MANAGE DMA.
16. U.S. Patent No. 5,671,355 to Collins entitled RECONFIGURABLE NETWORK INTERFACE APPARATUS AND METHOD
17. U.S. Patent No. 5,692,130 to Shobu et al. entitled METHOD FOR SELECTIVELY USING ONE OR TWO COMMUNICATION CHANNEL BY A TRANSMITTING DATA TERMINAL BASED ON DATA TYPE AND CHANNEL AVAILABILITY.
18. U.S. Patent No. 5,699,317 to Sartore et al. entitled ENHANCED DRAM WITH ALL READS FROM ON-CHIP CACHE AND ALL WRITERS TO MEMORY ARRAY.
19. U.S. Patent No. 5,701,434 to Nakagawa entitled INTERLEAVE MEMORY CONTROLLER WITH A COMMON ACCESS QUEUE.
20. U.S. Patent No. 5,749,095 to Hagersten entitled MULTIPROCESSING SYSTEM CONFIGURED TO PERFORM EFFICIENT WRITE OPERATIONS.
21. U.S. Patent No. 5,752,078 to Delp et al. entitled SYSTEM FOR MINIMIZING LATENCY DATA RECEPTION AND HANDLING DATA PACKET.
22. U.S. Patent No. 5,758,084 to Silverstein et al. entitled APPARATUS FOR PARALLEL CLIENT/SERVER COMMUNICATION HAVING DATA STRUCTURES WHICH STORED VALUES INDICATIVE OF A CONNECTION STATE AND ADVANCING THE CONNECTION STATE OF ESTABLISHED CONNECTIONS.
23. U.S. Patent No. 5,758,089 to Gentry et al. entitled METHOD AND APPARATUS FOR BURST TRANSFERRING ATM PACKET HEADER AND DATA TO A HOST COMPUTER SYSTEM.
24. U.S. Patent No. 5,758,186 to Hamilton et al. entitled METHOD AND APPARATUS FOR GENERICALLY HANDLING DIVERSE PROTOCOL METHOD CALLS IN A CLIENT/SERVER COMPUTER SYSTEM.

25. U.S. Patent No. 5,758,194 to Kuzma entitled COMMUNICATION APPARATUS FOR HANDLING NETWORKS WITH DIFFERENT TRANSMISSION PROTOCOLS BY STRIPPING OR ADDING DATA TO THE DATA STREAM IN THE APPLICATION LAYER.

26. U.S. Patent No. 5,790,804 to Osborne entitled COMPUTER NETWORK INTERFACE AND NETWORK PROTOCOL WITH DIRECT DEPOSIT MESSAGING.

27. U.S. Patent No. 5,812,775 to Van Seeters et al. entitled METHOD AND APPARATUS FOR INTERNETWORKING BUFFER MANAGEMENT.

28. PCT Pat. App. PCT/US97/17257 to Minami et al. entitled MULTIPLE NETWORK PROTOCOL ENCODER/DECODER AND DATA PROCESSOR.

29. Internet pages entitled Technical White Paper – Xpoint's Disk-to-LAN Acceleration Solution for Windows NT server, printed 6/5/97.

30. Jato Technologies Internet pages entitled Network Accelerator Chip Architecture, twelve-slide presentation, printed 8/19/98.

31. EETIMES article dated August 10, 1998, Issue 1020, entitled Enterprise system uses flexible spec, printed 11/25/98.

32. Internet pages entitled iREADY About Us and iREADY Products, printed 11/25/98.

33. Internet pages entitled Smart Ethernet Network Interface Card which Berend Ozceri is developing, and Internet pages entitled Hardware Assisted Protocol Processing, which Eugene Feinberg is working on, printed 11/25/98.

34. Internet pages of XaQti Corporation entitled GigaPOWER Protocol Processor Product Preview, printed 11/25/98.

Respectfully submitted,

Mark Lauer
Reg. No. 36,578
7041 Koll Center Parkway
Suite 280
Pleasanton, CA 94566
Tel: (925) 484-9295
Fax: (925) 484-9291

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 5, 1999.

Date: 1-5-99

Mark Lauer